



SINGLE BANK SDRAM TIMINGS

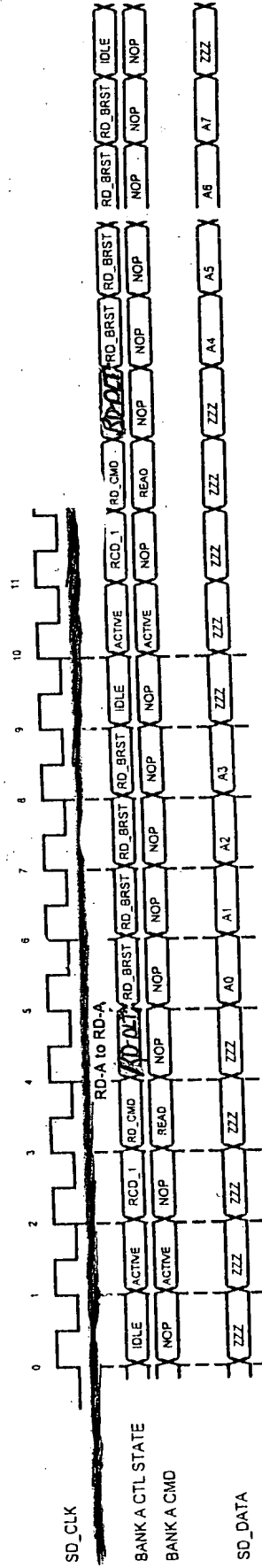


FIG. 15A

SINGLE BANK SDRAM TIMINGS

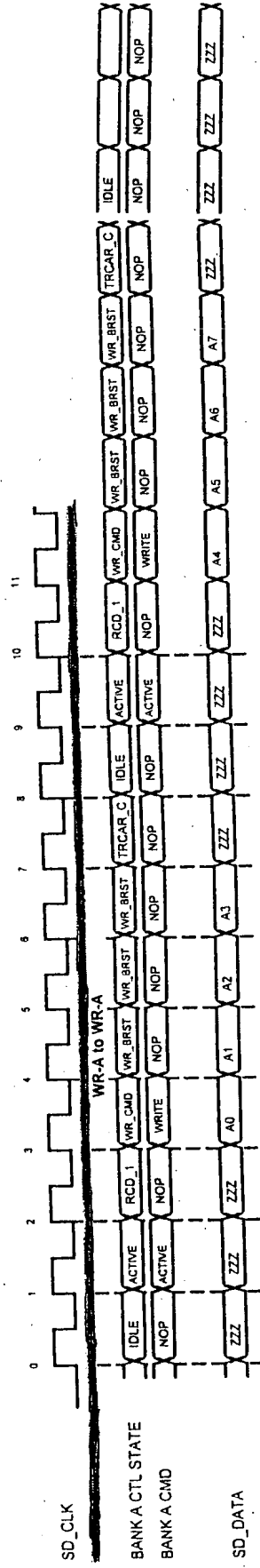


FIG. 15D

TWO BANK SDRAM TIMINGS

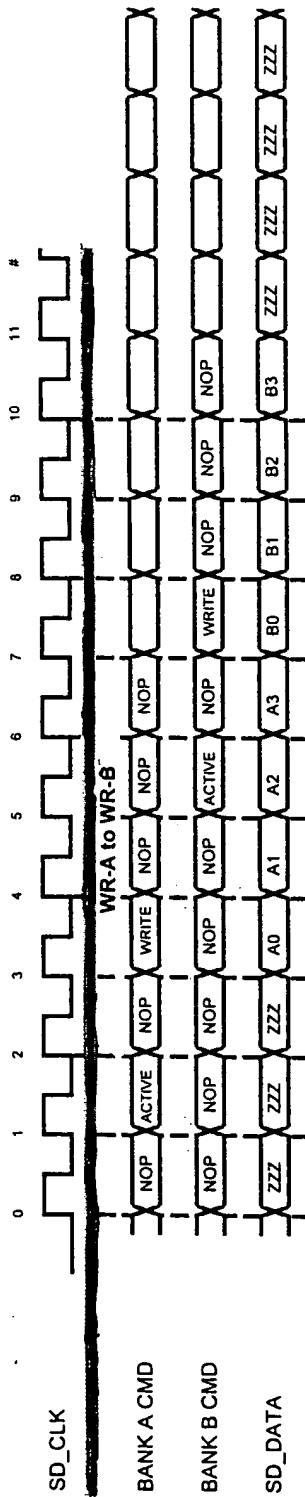


FIG. 16D